

Micro-Overlays for VPX

(Cost effective, high speed backplane, signal re-mapping) - By Brian Roberts

Overview:

Modern backplanes implement high speed signal standards like PCI Express, Serial Rapid I/O, SATA, SAS, and 10Gbit (XAUI) Ethernet. Backplanes need more flexibility to meet the wide variations in point to point differential pair connections specified by the VITA 46, cPCI Express, and pending VITA 65 (Open VPX) standards. The impedance variations and cost impact imposed by connectors like the VPX Mulitigig and cPCI Express ADF, cause significant challenges for standard overlay techniques that use these connectors. Connector-less Micro-overlays, present a Cost effective solution with the necessary signal integrity to meet this challenge.









Figure 3: Micro-overlay integration view.



Micro-overlays explained

Micro-overlays use BGA solder connection technology to interface a PCB based differential pair matrix with compatible backplanes. The "Micro" overlav reduces transmission line impedance variations and "stubs" associated with connector based interfaces by connecting directly to the main backplane via a solder interface. This technique improves the signal integrity between System cards beyond the requirements of the PCI Express, Serial Rapid I/O, and 10Gbit (XAUI) Ethernet standards. Micro-overlays also allow standard stock Dawn backplanes to be customized to the client requirements, without the need for new backplane designs. This is shown in Figure1. Micro-overlays can also facilitate rear transition modules and low profile connector interface systems when normal transition modules do not fit the system application envelope. Dawn's Micro-overlays also provides a natural migratory development environment for moving from the lab to the field with the same high speed backplanes due to the rugged , low mass, connector-less implementation of Micro-overlavs.

(This feature is unique to Dawn Backplanes and is patent pending)

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